

**SPECIFICATION  
FOR  
LCD Module  
KD032QVTMA011-RT**

<b>MODULE:</b>	<b>KD032QVTMA011-RT</b>
<b>CUSTOMER:</b>	

<b>REV</b>	<b>DESCRIPTION</b>	<b>DATE</b>
<b>1.0</b>	<b>FIRST ISSUE</b>	<b>2015.12.02</b>
<b>1.1</b>	<b>更改FPC长度</b>	<b>2016.07.20</b>

<b>STARTEK</b>	<b>INITIAL</b>	<b>DATE</b>
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<b>CHECKED BY</b>		
<b>APPROVED BY</b>		

<b>CUSTOMER</b>	<b>INITIAL</b>	<b>DATE</b>
<b>APPROVED BY</b>		



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## General Description

### \* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.2" TFT-LCD contains 240x320 pixels, and can display up to 65K/262K colors.

### \* Features

- Low Input Voltage: 3.3V (TYP)
- Display Colors of TFT LCD: 65K/262K colors
- Interface: 18/16/9/8 BIT MCU
  - 3/4-line Serial
  - 16/18BIT RGB

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.60(H)*64.80(V) (3.2inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.2025(H)*0.2025(V)	mm	-
Viewing angle	6:00	o'clock	-
Controller IC	ST7789V	-	-
Display mode	Transmissive/Normally White	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

### \* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		55.00		mm	-
	Vertical(V)		77.20		mm	-
	Depth(D)		2.60		mm	-
Weight			TBD		g	-

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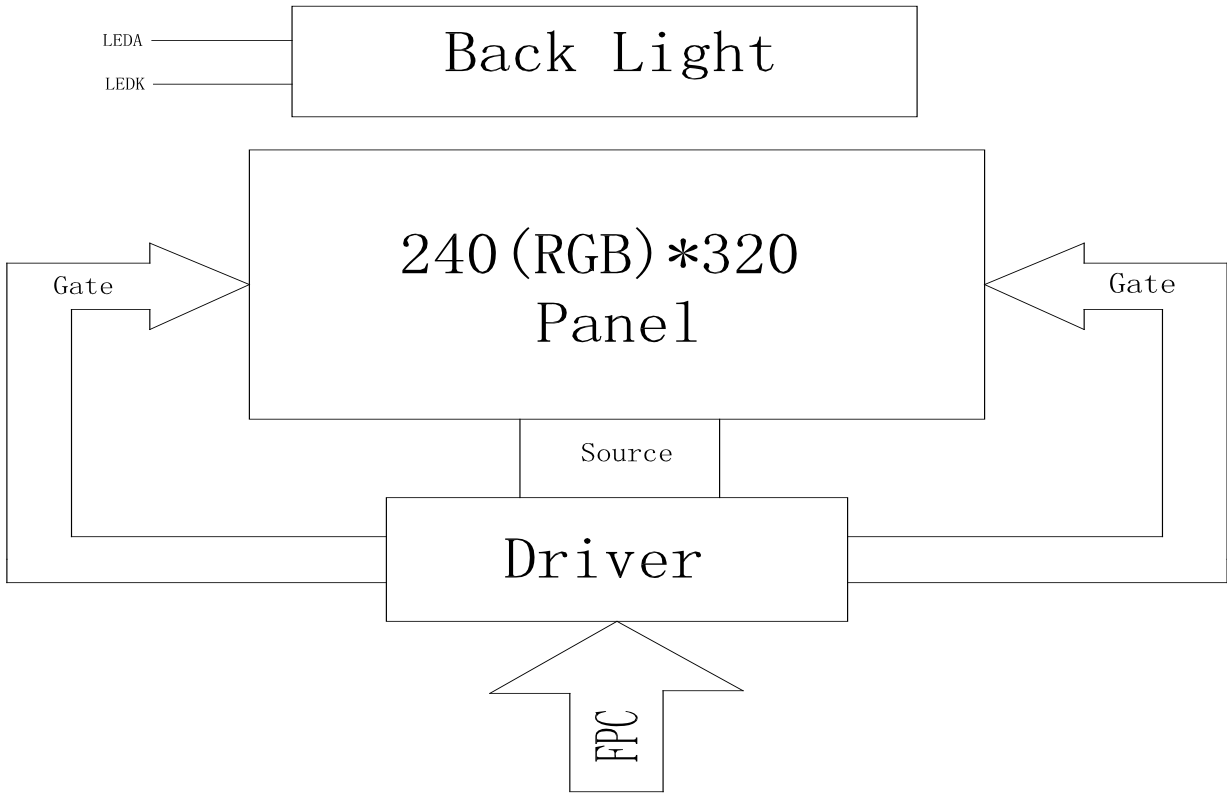
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1. Block Diagram



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### 3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	XR	Touch panel Right Glass Terminal.	A/D
3	YD	Touch panel Bottom Film Terminal.	A/D
4	XL	Touch panel LIFT Glass Terminal.	A/D
5	YU	Touch panel Top Film Terminal.	A/D
6	IOVCC	Supply voltage for IO (1.8-3.3V).	P
7	IOVCC	Supply voltage for IO (1.8-3.3V).	P
8	VCI	Supply voltage (3.3V).	P
9	VCI	Supply voltage (3.3V).	P
10	IM2	-MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. -Fix this pin at VCI and GND.	I
11	IM1		
12	IM0		
13	RESET	-This signal will reset the device and must be applied to properly initialize the chip.	I
14	CS	-Chip select input pin ("Low" enable). -Fix this pin at VCI or GND when not in use.	I
15	RS(SPI-SCL)	-This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected.  This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. -Fix this pin at VCI or GND when not in use.	I
16	WR(SPI-RS)	-The data is applied on the rising edge of the SCL signal. -Fix this pin at VCI or GND when not in use.	I
17	RD	-Serves as a read signal and MCU read data at the rising edge. -Fix this pin at VCI or GND when not in use	I
18	VSYNC	-Frame synchronizing signal for RGB interface operation. -Fix this pin at VCI or GND when not in use.	I



19	HSYNC	-Line synchronizing signal for RGB interface operation. -Fix this pin at VCI or GND when not in use.	I
20	ENABLE	-Data enable signal for RGB interface operation. -Fix this pin at VCI or GND when not in use.	I
21	DOTCLK	-Dot clock signal for RGB interface operation. -Fix this pin at VCI or GND when not in use.	I
22	SDA	-Serial input signal. The data is applied on the rising edge of the SCL signal. -If not used, fix this pin at VCI or GND.	I
23-40	DB[0:17]	-DB[17:0] are used as MCU parallel interface data bus. 8-bit I/F: when IM3:0, DB[7:0] are used; when IM3:1, DB[17:10] are used. 9-bit I/F: when IM3:0, DB[8:0] are used; when IM3:1, DB[17:9] are used. 16-bit I/F: when IM3:0, DB[15:0] are used; when IM3:1, DB[17:10] and DB[8:1] are used. 18-bit I/F: DB[17:0] are used. -DB[17:0] are used as RGB interface data bus. 16-bit RGB I/F: DB[17:13], DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. -If not used, please fix this pin at VDDI or DGND.	I/O
41	SDO	-SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
42	GND	Ground.	P
43	LEDA	Anode pin of backlight	P
44	LEDK1	Cathode pin OF backlight	P
45	LEDK2	Cathode pin OF backlight	P
46	LEDK3	Cathode pin OF backlight	P
47	LEDK4	Cathode pin OF backlight	P
48	LEDK5	Cathode pin OF backlight	P
49	LEDK6	Cathode pin OF backlight	P
50	GND	Ground.	P



## 4. LCD Optical Characteristics

### 4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Transmittance (with Polarizer)	T(%)	--	--	18.0	--	%	Note1
Contrast Ratio	CR	$\theta=0$	400	500		%	(1)(2)
Response time	Rising	Normal viewing angle	--	4	8	msec	(1)(3)
	Falling		--	12	24		
Color gamut	S(%)		--	60	--	%	Note5
Color Filter Chromaticity	White	$W_X$	0.283	0.303	0.323		(1)(4) CF glass (C-light)
		$W_Y$	0.305	0.325	0.345		
	Red	$R_X$	0.606	0.626	0.646		
		$R_Y$	0.314	0.334	0.354		
	Green	$G_X$	0.257	0.277	0.297		
		$G_Y$	0.529	0.549	0.569		
	Blue	$B_X$	0.122	0.142	0.162		
		$B_Y$	0.102	0.122	0.142		
Viewing angle	Hor.	$\theta_L$	50	70	--	Degree	Note 2
		$\theta_R$	50	70	--		
	Ver.	$\theta_U$	60	75	--		
		$\theta_D$	40	50	--		
Option View Direction	6 O'clock						

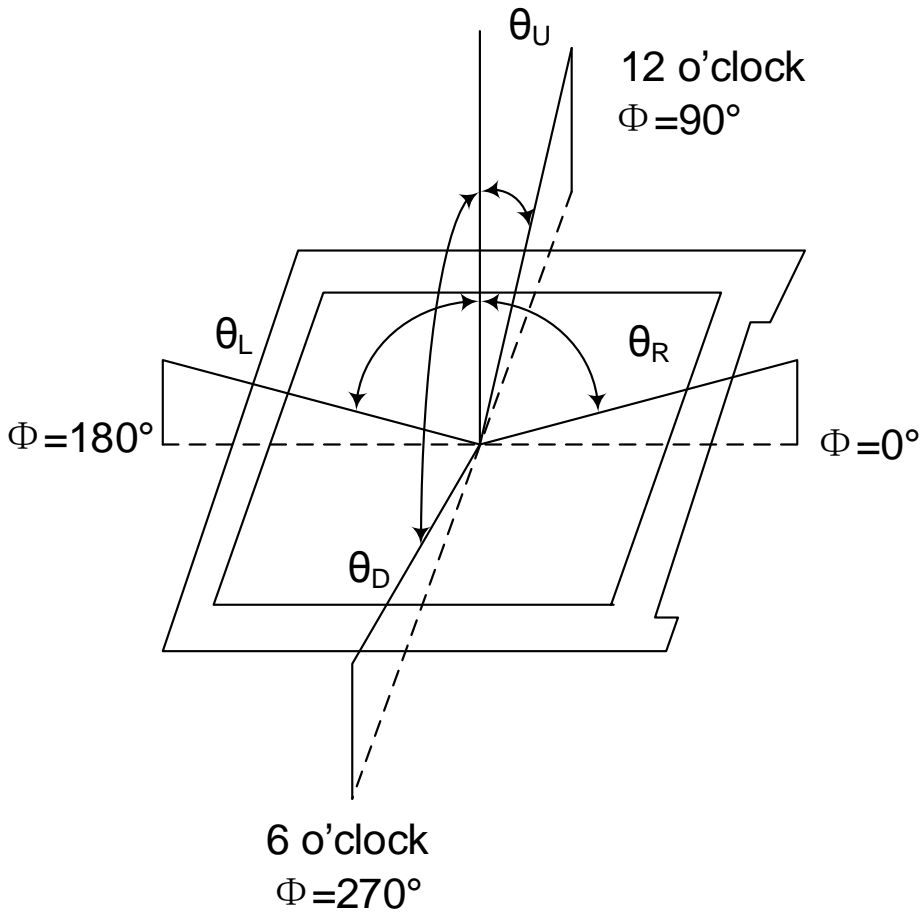
### 4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature:  $25\pm 2^{\circ}\text{C}$
- 15min. warm-up time.

### 4.3 Measuring Equipment

■ FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

**Note (1)** Definition of Viewing Angle :

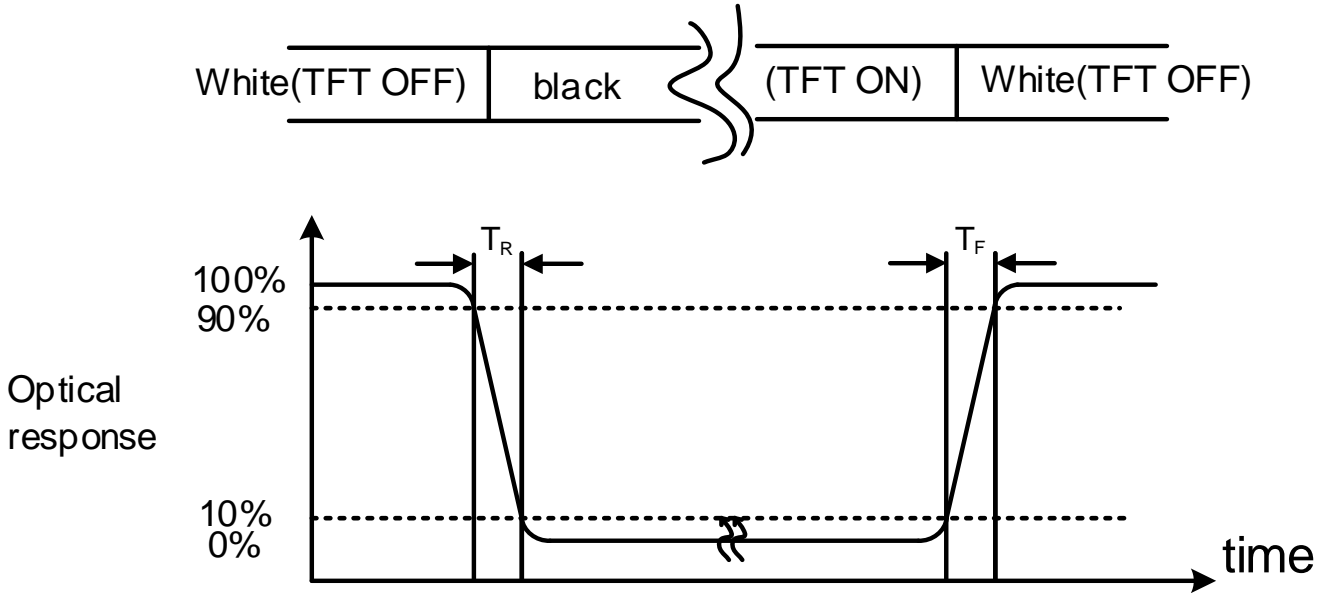


**Note (2)** Definition of Contrast Ratio (CR) :

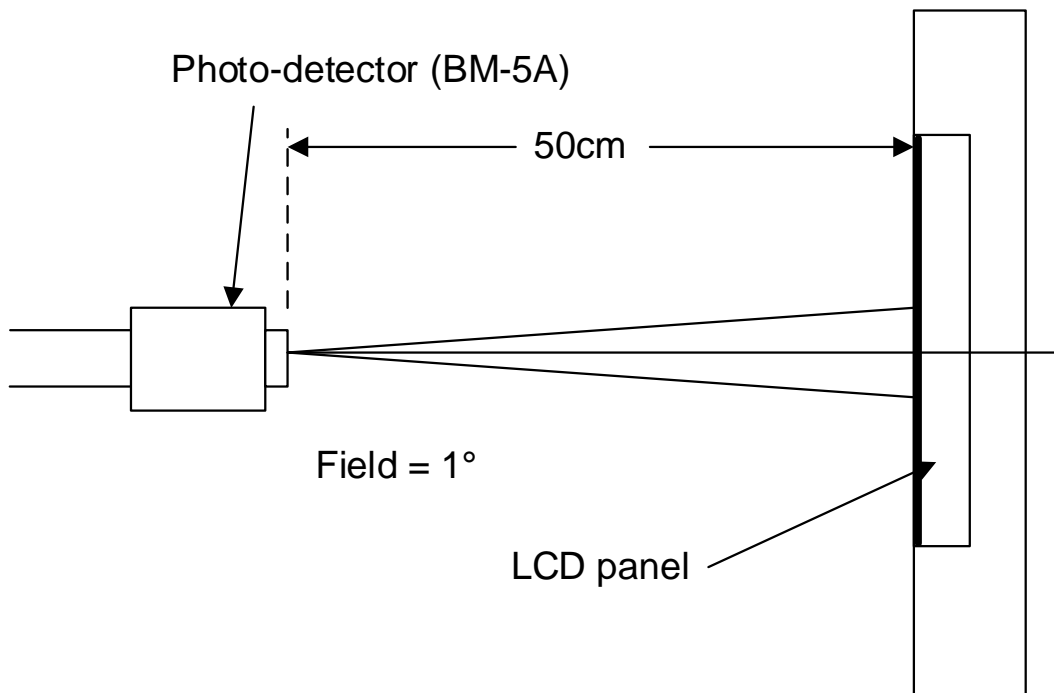
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

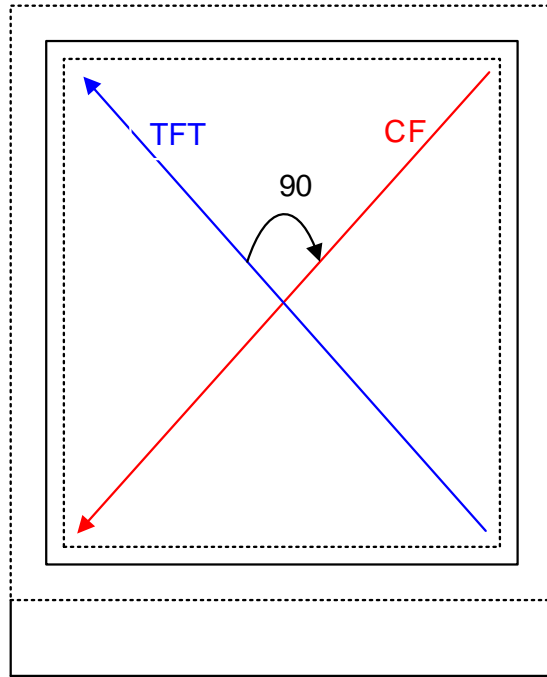
**Note (3)** Definition of Response Time: Sum of TR and TF



**Note (4)** Definition of optical measurement setup



**Note (5)** Rubbing Direction (The different Rubbing Direction will cause the different view direction.



TFT Face up

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## 5. Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.8	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

### 5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.4	3.3	4.8	V	
Digital interface supply Voltage	VDDIO	1.65	3.3	4.8	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V <sub>IH</sub>	0.7V <sub>DDIO</sub>		V <sub>DDIO</sub>	V	
	V <sub>IL</sub>	GND		0.3V <sub>DDIO</sub>	V	
Level output voltage	V <sub>OH</sub>	0.8V <sub>DDIO</sub>		V <sub>DDIO</sub>	V	
	V <sub>OL</sub>	GND		0.2V <sub>DDIO</sub>	V	

### 5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I <sub>F</sub>	90	120	--	mA	
Forward Voltage	V <sub>F</sub>	--	3.2	--	V	
LCM Luminance	L <sub>V</sub>	350	--	--	cd/m <sup>2</sup>	I <sub>f</sub> =60mA

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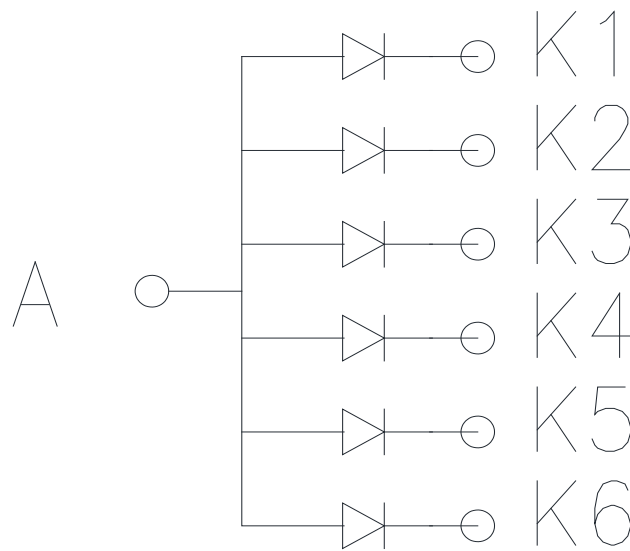
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LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm3\text{ }^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at  $T_a=25\text{ }^\circ\text{C}$  and  $I_L=120\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 120mA. The constant current driving method is suggested.



## BL CURCUIT DIAGRAM

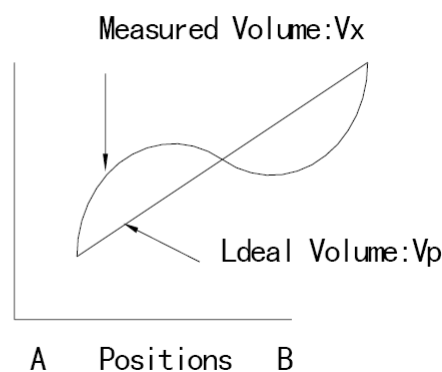
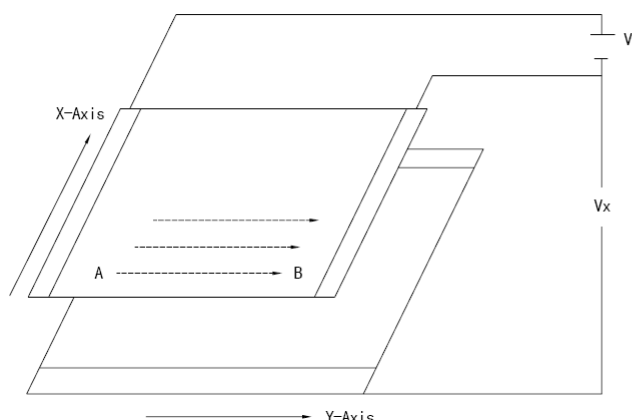
## 6. TP Feature

### 6.1 Conditions of use and storage

Item	Value(condition)	Note
Temperature range upon operation	Humidity: 20%~90% non dew, condensation -20°C~70°C	In a simple substance
Temperature range upon storage	Humidity: 20%~90% non dew, condensation -30°C~80°C	In a simple substance

### 6.2 Electrical property

Item	Value	Note
Maximum voltage	DC5V	
Resistance between terminals	X direction[Film side]:200-600Ω	
	Y direction [Glass side]:300-900Ω	
Insulation resistance	DC 25V 20MΩor above	Connect X + ~X- and Y+ ~Y-, apply 25VDC Between X and Y for perform measurements
Chattering	10 msec or below	
Rating	Voltage is DC 5V	



### 6.3 Mechanical property

Item	Performance		Note
Input method	Used of an exclusive pen or finger		
Load upon operation	Exclusive pen	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: s: Stylus pen material: POM (polyacetal). Tip : Diameter 3.0mm, SR 0.8 mm
	Finger	60-100g or below	Operations and measurement methods simulated for a finger must be carried out under the following tip conditions. Material :Silicon rubber (Hardness : 30°Hs) Tip : Diameter 12.0 mm, SR 12.5mm
Surface hardness	Pencil hardness : 3H or above		It complies with the way of test method JIS K5400.

### 6.4 Optical property

Item	Performance	Note
Total light transmittance	80% or above	JIS K7105
Haze	5% or below	JIS K7136
Film specification	Polished type with hard coated surface	



## 7. AC Characteristic

### 7.1. 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

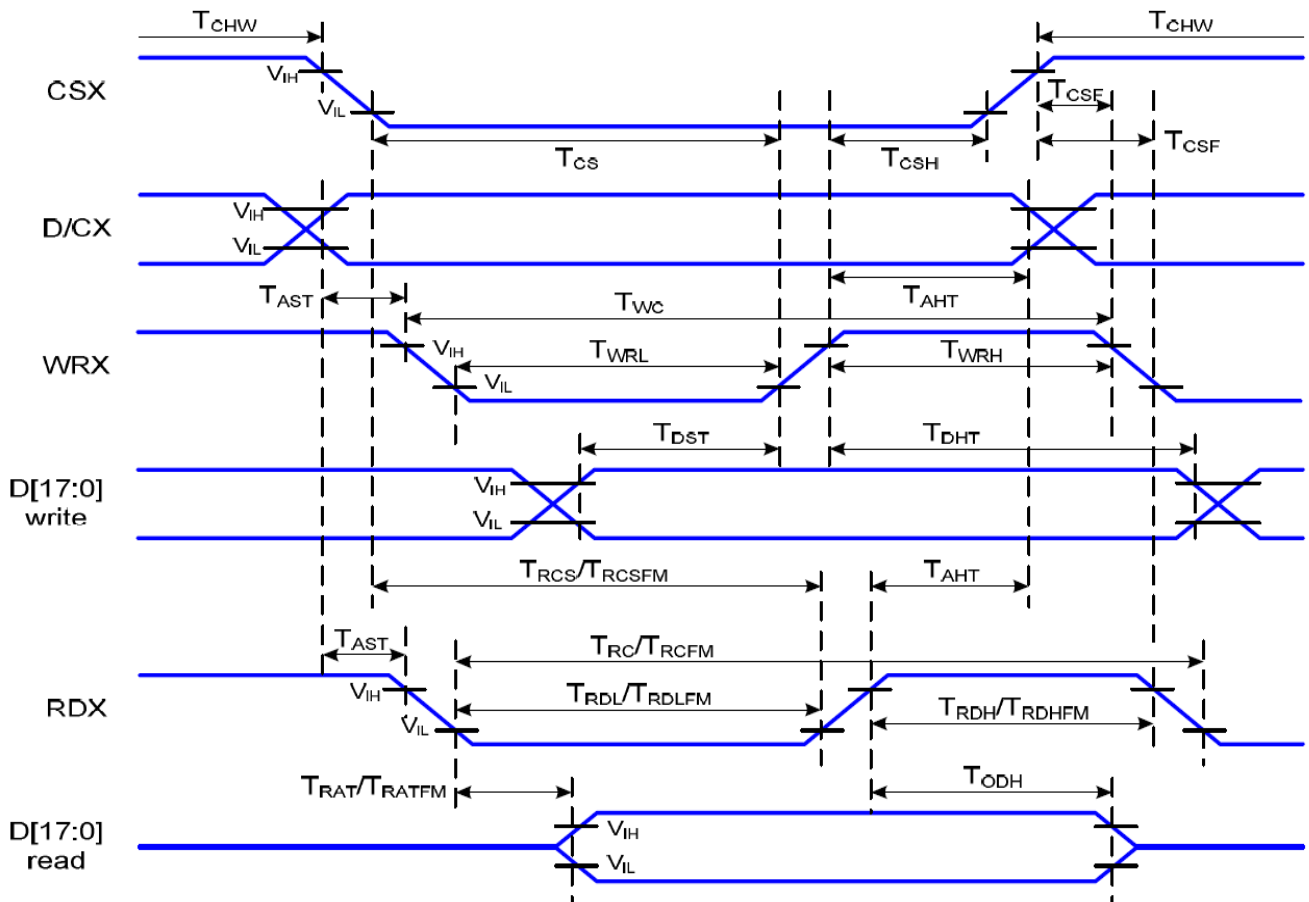


Figure6-1-1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

$V_{DDI}=1.65$  to  $3.3V$ ,  $V_{DD}=2.4$  to  $3.3V$ ,  $AGND=DGND=0V$ ,  $T_a=-30$  to  $70$  °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	$T_{AST}$	Address setup time	0		ns	
	$T_{AHT}$	Address hold time (Write/Read)	10		ns	
CSX	$T_{CHW}$	Chip select "H" pulse width	0		ns	
	$T_{CS}$	Chip select setup time (Write)	15		ns	
	$T_{RCS}$	Chip select setup time (Read ID)	45		ns	
	$T_{RCSFM}$	Chip select setup time (Read FM)	355		ns	
	$T_{CSF}$	Chip select wait time (Write/Read)	10		ns	
	$T_{CSH}$	Chip select hold time	10		ns	
WRX	$T_{WC}$	Write cycle	66		ns	

	$T_{WRH}$	Control pulse "H" duration	15		ns	
	$T_{WRL}$	Control pulse "L" duration	15		ns	
RDX(ID)	$T_{RC}$	Read cycle (ID)	160		ns	When read ID data
	$T_{RDH}$	Control pulse "H" duration (ID)	90		ns	
	$T_{RDL}$	Control pulse "L" duration (ID)	45		ns	
RDX(FM)	$T_{RCFM}$	Read cycle (FM)	450		ns	When read from frame memory
	$T_{RDHFM}$	Control pulse "H" duration(FM)	90		ns	
	$T_{RDLFM}$	Control pulse "L" duration(FM)	355		ns	
DB[17:0]	$T_{DST}$	Data setup time	10		ns	For CL=30pF
	$T_{DHT}$	Data hold time	10		ns	
	$T_{RAT}$	Read access time (ID)		40	ns	
	$T_{RATFM}$	Read access time (FM)		340	ns	
	$T_{ODH}$	Output disable time	20	80	ns	

Table6-1-1 8080 Parallel Interface Characteristics

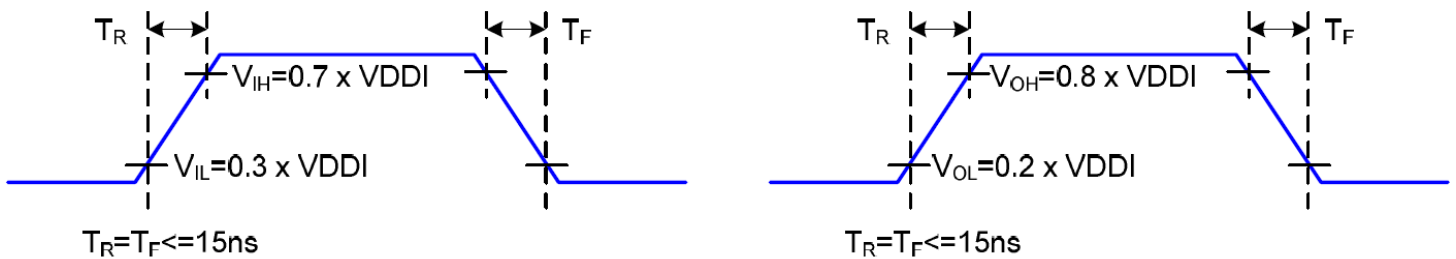


Figure6-1-2 Rising and Falling Timing for I/O Signal

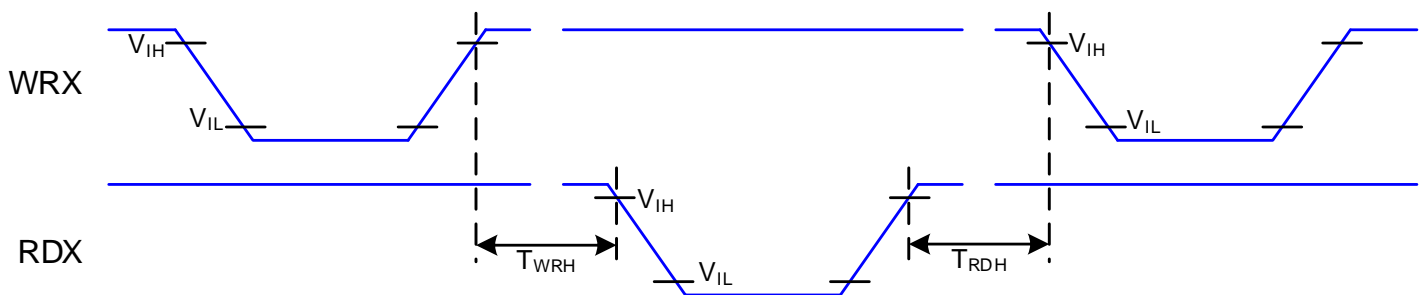


Figure6-1-3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

### 7.2. Serial Interface Characteristics (3-line serial):

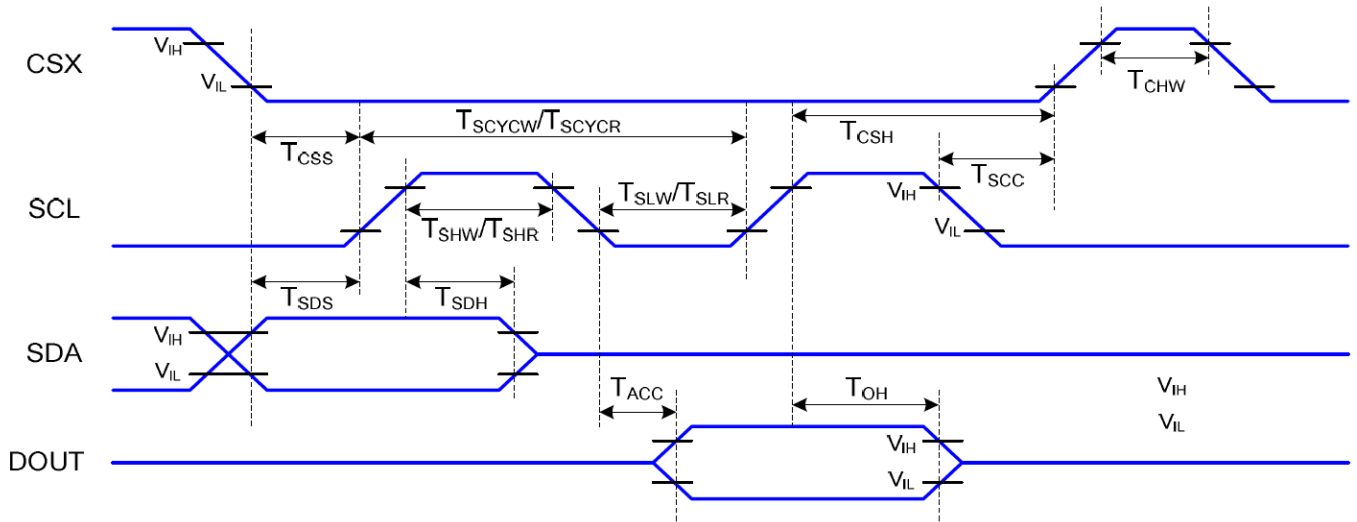


Figure6-2-1 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time (Write)	15		ns	
	T <sub>CSH</sub>	Chip select hold time (write)	15		ns	
	T <sub>CSS</sub>	Chip select setup time (read)	60		ns	
	T <sub>SCC</sub>	Chip select hold time (read)	65		ns	
	T <sub>CHW</sub>	Chip select "H" pulse width	40		ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle (Write)	66		ns	
	T <sub>SHW</sub>	SCL "H" pulse width (Write)	15		ns	
	T <sub>SLW</sub>	SCL "L" pulse width (Write)	15		ns	
	T <sub>SCYCR</sub>	Serial clock cycle (Read)	150		ns	
	T <sub>SHR</sub>	SCL "H" pulse width (Read)	60		ns	
	T <sub>SLR</sub>	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T <sub>SDS</sub>	Data setup time	10		ns	
	T <sub>SDH</sub>	Data hold time	10		ns	
DOUT	T <sub>ACC</sub>	Access time	10	50	ns	For maximum CL=30pF
	T <sub>OH</sub>	Output disable time	15	50	ns	For minimum CL=8pF

Table6-2-1 3-line serial Interface Characteristics

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

### 7.3. Serial Interface Characteristics (4-line serial):

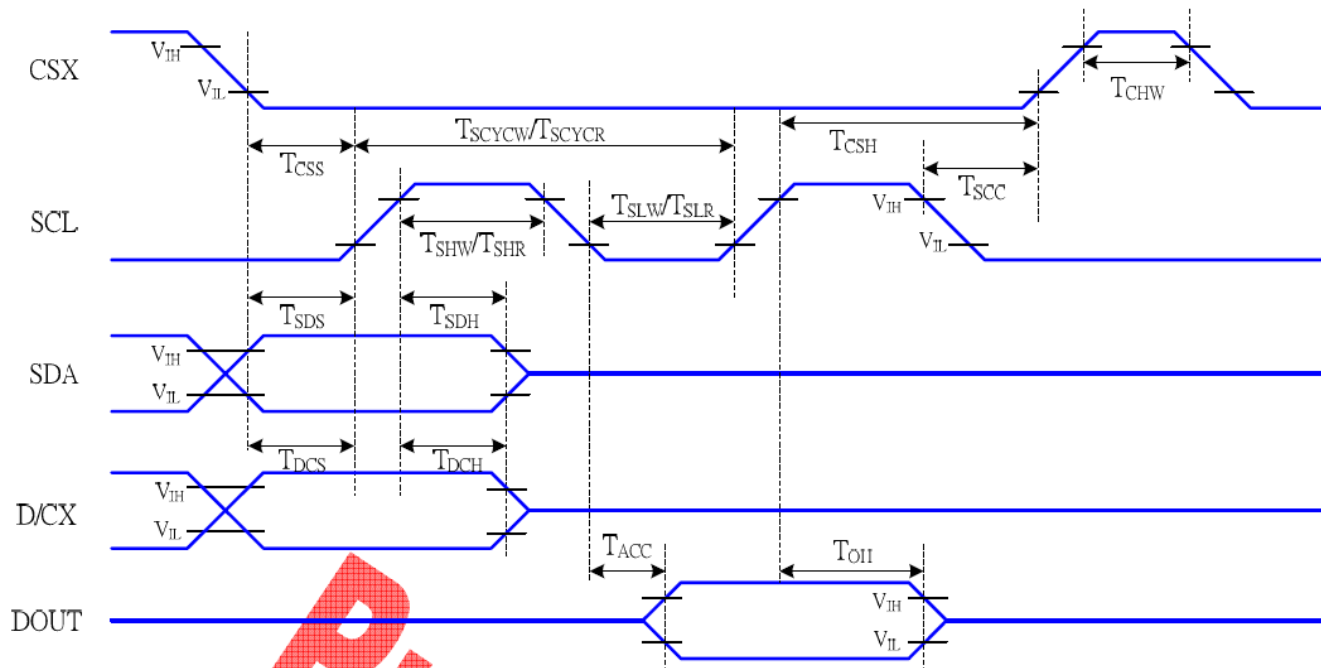


Figure6-3-1 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V,  $T_a = -30$  to  $70$  °C

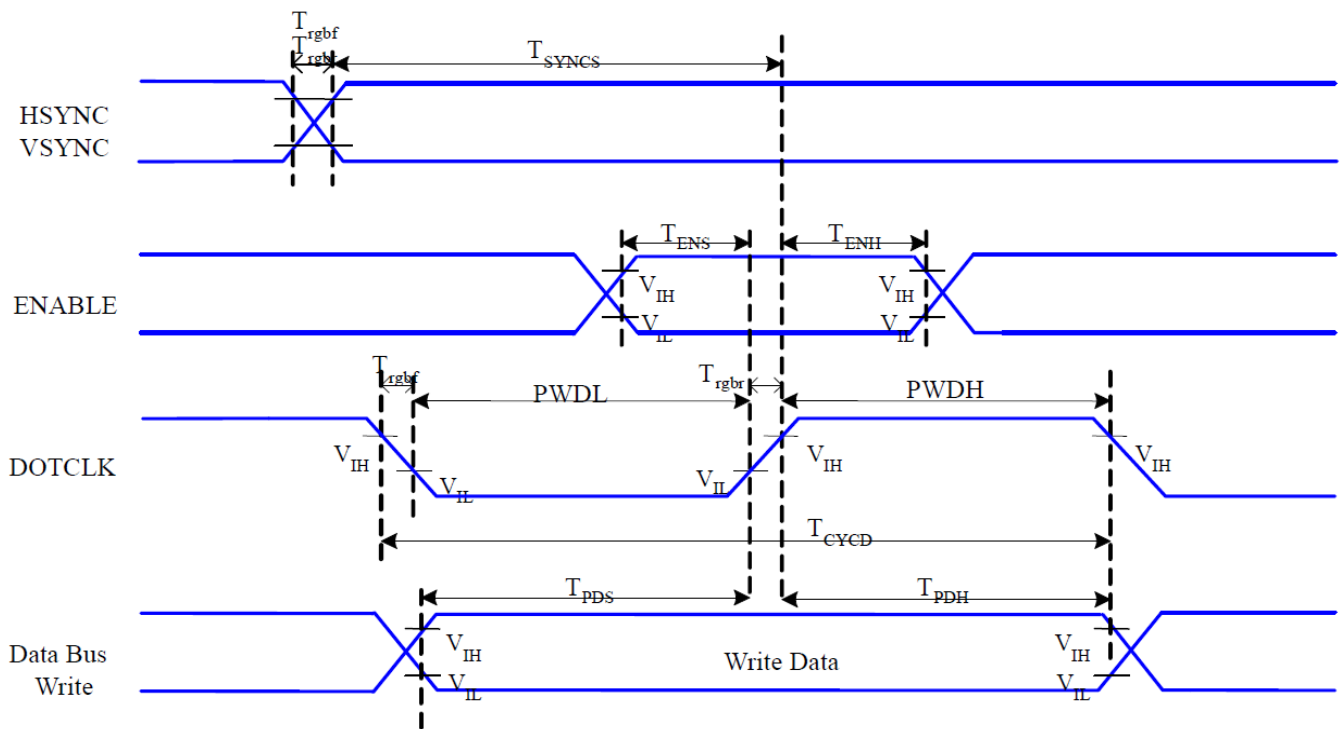
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	$T_{CSS}$	Chip select setup time (Write)	15		ns	
	$T_{CSH}$	Chip select hold time (write)	15		ns	
	$T_{CSS}$	Chip select setup time (read)	60		ns	
	$T_{SCC}$	Chip select hold time (read)	65		ns	
	$T_{CHW}$	Chip select "H" pulse width	40		ns	
SCL	$T_{SCYCW}$	Serial clock cycle (Write)	66		ns	-write command & data ram
	$T_{SHW}$	SCL "H" pulse width (Write)	15		ns	
	$T_{SLW}$	SCL "L" pulse width (Write)	15		ns	
	$T_{SCYCR}$	Serial clock cycle (Read)	150		ns	-read command & data ram
	$T_{SHR}$	SCL "H" pulse width (Read)	60		ns	
	$T_{SLR}$	SCL "L" pulse width (Read)	60		ns	
D/CX	$T_{DCS}$	D/CX setup time	10		Ns	
	$T_{DCH}$	D/CX hold time	10		ns	

SDA (DIN)	$T_{SDS}$	Data setup time	10		ns	
	$T_{SDH}$	Data hold time	10		ns	
DOUT	$T_{ACC}$	Access time	10	50	ns	For maximum CL=30pF
	$T_{OH}$	Output disable time	15	50	ns	For minimum CL=8pF

**Table6-2-1 4-line serial Interface Characteristics**

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

### 7.4. RGB Interface Characteristics:



**Figure6-4-1 RGB Interface Timing Characteristics**

$VDDI=1.65$  to  $3.3V$ ,  $VDD=2.4$  to  $3.3V$ ,  $AGND=DGND=0V$ ,  $T_a=-30$  to  $70$  °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	$T_{SYNCS}$	VSYNC, HSYNC Setup Time	30		ns	
ENABLE	$T_{ENS}$	Enable Setup Time	25		ns	
	$T_{ENH}$	Enable Hold Time	25		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60		ns	
	PWDL	DOTCLK Low-level Pulse Width	60		ns	

	$T_{CYCD}$	DOTCLK Cycle Time	120		ns
	$T_{rghr}$ $T_{rghf}$	DOTCLK Rise/Fall time		20	ns
DB	$T_{PDS}$	PD Data Setup Time	50		ns
	$T_{PDH}$	PD Data Hold Time	50		ns

Table6-4-1 18/16 Bits RGB Interface Timing Characteristics

### 7.5 Reset Timing Characteristics

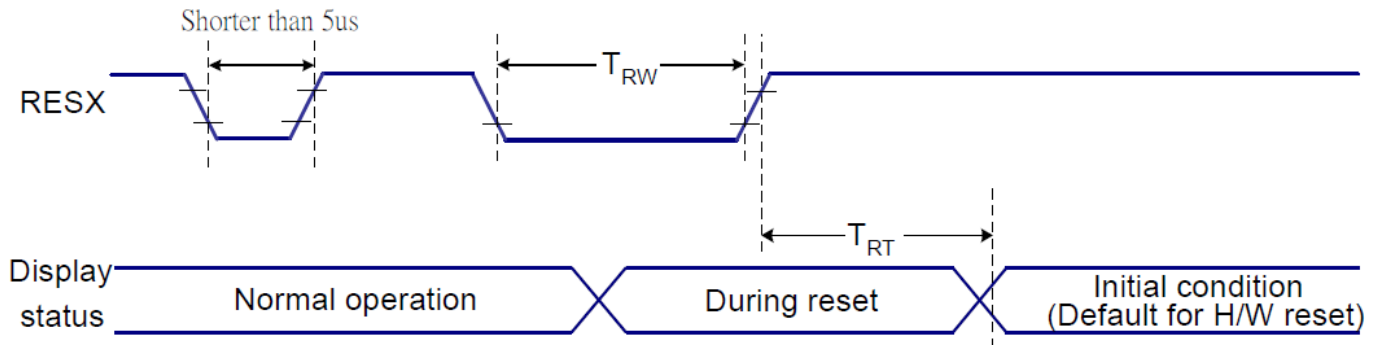


Figure6-5-1 Reset Timing

$V_{DDI}=1.65$  to  $3.3V$ ,  $V_{DD}=2.4$  to  $3.3V$ ,  $AGND=DGND=0V$ ,  $T_a=-30$  to  $70$  °C

Signal	Symbol	Parameter	Min	Max	Unit
RESX	$T_{RW}$	Reset pulse duration	10		us
	$T_{RT}$	Reset cancel		5 (Note 1, 5) 120 (Note 1, 6, 7)	ms ms

Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.)

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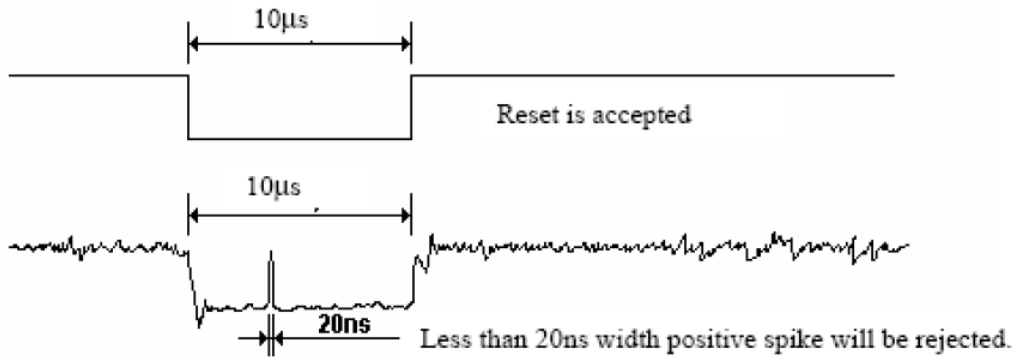
期 供   
Long Availability

支持小量  
NO MOQ

品   全  
In Full Range

and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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	常 □ □ 存 Standing Stock	□ 期 供 □ Long Availability	支持小量 NO MOQ	品 □ □ 全 In Full Range

## 8. LCD Module Out-Going Quality Level

### 8.1 VISUAL & FUNCTION INSPECTION STANDARD

#### 8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

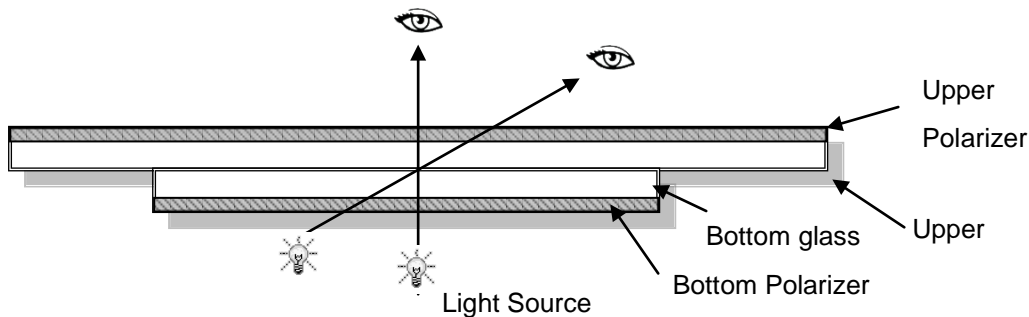
Temperature:  $25\pm 5^{\circ}\text{C}$

Humidity:  $65\%\pm 10\%\text{RH}$

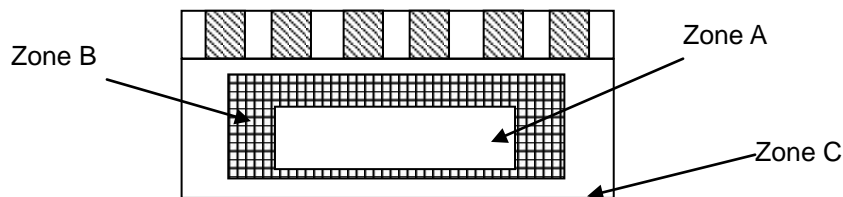
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



#### 8.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen).

Zone B: Viewing Area except Zone A.

Zone C: Outside (Zone A + Zone B) which can't be seen after assembly by customer.

Note:

As a general rule, visual defects in Zone C can be ignored when it doesn't effecting product function or appearance after assembly by customer.

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### 8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

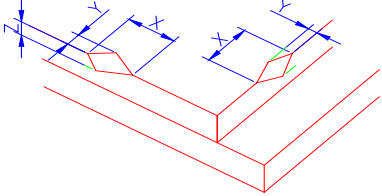
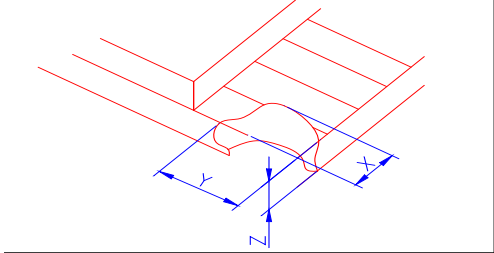
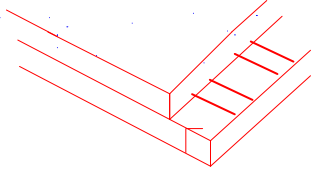
AQL:

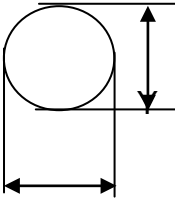
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

### 8.1.4 Criteria (Visual)

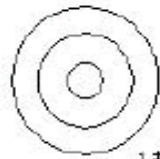


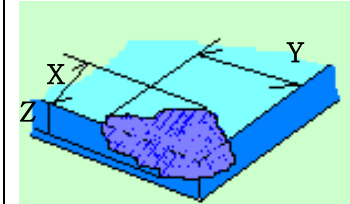
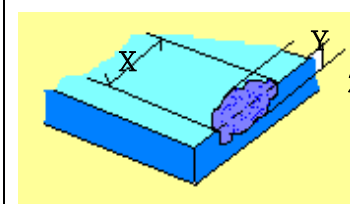
Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken  NOTE: X: Length Y: Width Z: Height L:Length of ITO T:Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="868 647 1441 797"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td>&lt;Inner border line of the seal</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
	(2)LCD corner broken	 <table border="1" data-bbox="932 1160 1377 1261"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>						

Number	Items	Criteria (mm)																				
2.0	Spot defect  $\Phi = (X+Y)/2$	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain) <table border="1" data-bbox="454 459 1316 817"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Quality</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.10</math></td> <td colspan="2">Ignore</td> <td rowspan="4">Ignor</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.25</math></td> <td colspan="2">3( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>0.25 &lt; \Phi \leq 0.40</math></td> <td colspan="2">2</td> </tr> <tr> <td><math>\Phi &gt; 0.40</math></td> <td colspan="2">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Quality			A	B	C	$\Phi \leq 0.10$	Ignore		Ignor	$0.10 < \Phi \leq 0.25$	3( distance $\geq 10\text{mm}$ )		$0.25 < \Phi \leq 0.40$	2		$\Phi > 0.40$	0	
		Zone Size (mm)		Acceptable Quality																		
			A	B	C																	
		$\Phi \leq 0.10$	Ignore		Ignor																	
		$0.10 < \Phi \leq 0.25$	3( distance $\geq 10\text{mm}$ )																			
		$0.25 < \Phi \leq 0.40$	2																			
		$\Phi > 0.40$	0																			
		② Dim spot (LCD/TP/Polarizer dim dot, light leakage、 dark spot) <table border="1" data-bbox="454 862 1316 1220"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Quality</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.1</math></td> <td colspan="2">Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.25</math></td> <td colspan="2">3( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>0.25 &lt; \Phi \leq 0.40</math></td> <td colspan="2">2</td> </tr> <tr> <td><math>\Phi &gt; 0.40</math></td> <td colspan="2">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Quality			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.10 < \Phi \leq 0.25$	3( distance $\geq 10\text{mm}$ )		$0.25 < \Phi \leq 0.40$	2		$\Phi > 0.40$	0	
		Zone Size (mm)		Acceptable Quality																		
			A	B	C																	
		$\Phi \leq 0.1$	Ignore		Ignore																	
		$0.10 < \Phi \leq 0.25$	3( distance $\geq 10\text{mm}$ )																			
$0.25 < \Phi \leq 0.40$	2																					
$\Phi > 0.40$	0																					
③ Polarizer accidented spot <table border="1" data-bbox="454 1265 1316 1556"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Quality</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.2</math></td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td><math>0.2 &lt; \Phi \leq 0.5</math></td> <td colspan="2">2( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>\Phi &gt; 0.5</math></td> <td colspan="2">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Quality			A	B	C	$\Phi \leq 0.2$	Ignore		Ignore	$0.2 < \Phi \leq 0.5$	2( distance $\geq 10\text{mm}$ )		$\Phi > 0.5$	0						
Zone Size (mm)		Acceptable Quality																				
	A	B	C																			
$\Phi \leq 0.2$	Ignore		Ignore																			
$0.2 < \Phi \leq 0.5$	2( distance $\geq 10\text{mm}$ )																					
$\Phi > 0.5$	0																					

Line defect (LCD/TP /Polarizer black/white line, scratch, stain)		Acceptable Quality		
	Width(mm)	Length(mm)	A	B
	$\Phi \leq 0.03$	Ignore	Ignore	
	$0.03 < W \leq 0.05$	$L \leq 3.0$	$N \leq 2$	
	$0.05 < W \leq 0.08$	$L \leq 2.0$	$N \leq 2$	
	$0.08 < W$	Define as spot defect		

3.0	Polarizer Bubble	Zone	Acceptable Qty		
		Size (mm)	A	B	C
		$\Phi \leq 0.2$	Ignore		Ignore
		$0.2 < \Phi \leq 0.4$	3 (distance $\geq 10 \square m$ )		
		$0.4 < \Phi \leq 0.6$	2		
$0.6 < \Phi$	0				
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.			

5.0	TP Related	TP bubble/ accidented spot	Size $\Phi$ (mm)	Acceptable Qty		
			$\Phi \leq 0.1$	A	B	C
			$0.1 < \Phi \leq 0.25$	Ignore		Ignore
			$0.25 < \Phi \leq 0.3$	3 (distance $\geq$		
			$0.3 < \Phi$	2		
			0			
	Assembly deflection	beyond the edge of backlight $\leq 0.15mm$				

			<p>Newton Ring area &gt; 1/3 TP area NG</p> <p>Newton Ring area ≤ 1/3 TP area OK</p>	 1 规律性  2 非规律性  似牛顿环						
		<p>TP corner broken</p> <p>X : length Y : width Z : height</p>	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>X ≤ 3.0mm</td> <td>Y ≤ 3.0mm</td> <td>Z &lt; LCD thickness</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	X ≤ 3.0mm	Y ≤ 3.0mm	Z < LCD thickness	
X	Y	Z								
X ≤ 3.0mm	Y ≤ 3.0mm	Z < LCD thickness								
		<p>TP edge broken</p> <p>X : length Y : width Z : height</p>	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>X ≤ 6.0mm</td> <td>Y ≤ 2.0mm</td> <td>Z &lt; LCD thickness</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	X ≤ 6.0mm	Y ≤ 2.0mm	Z < LCD thickness	
X	Y	Z								
X ≤ 6.0mm	Y ≤ 2.0mm	Z < LCD thickness								

Criteria ( functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

## 9. Reliability Test Result

### 9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70°C90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	- 30°C, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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常 <input type="checkbox"/> 存 Standing Stock		<input type="checkbox"/> 期 供 <input type="checkbox"/> Long Availability		支持小量 NO MOQ
品 <input type="checkbox"/> 全 In Full Range				

## 10. Cautions and Handling Precautions

### 10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.  
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.  
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.  
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

### 10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.  
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.  
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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	常 <input type="checkbox"/> <input type="checkbox"/> 存 Standing Stock	<input type="checkbox"/> 期 供 <input type="checkbox"/> Long Availability	支持小量 NO MOQ	品 <input type="checkbox"/> <input type="checkbox"/> 全 In Full Range

## 11 Packing

----TBD-----

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	常 <input type="checkbox"/> <input type="checkbox"/> 存 Standing Stock	<input type="checkbox"/> 期 供 <input type="checkbox"/> Long Availability	支持少量 NO MOQ	品 <input type="checkbox"/> <input type="checkbox"/> 全 In Full Range